REMARKS

This is in response to the Office Action dated March 3, 2004. In that Office Action Examiner rejected claims 1-16 (all the claims) on various grounds. Examiner also objected to the drawings under 37CFR1.83(a). A new proposed drawing and Letter to the Chief Draftsman are enclosed herewith. The drawing now identifies SiGe as the substrate material. Extensive support for this drawing modification is found in the specification, for example at page 2, line 9, page 3 lines 19-21, and page 4, line 3. The drawing now shows microprocessor 300 connected at two sites to output pads 120 and 130. Extensive support for this drawing modification is found, for example, in the Abstract and at page 2 lines 4, 12, 13, 15 and 27, and page 4 lines 2-15 and 27. In this regard, the specification has been amended to add a reference numeral identifying microprocessor 300. The remaining objections to the drawings are believed to be moot because claims 6 and 14, which were referenced in the drawing rejection, have been canceled.

The Examiner rejected claim 5 under the provisions of 35USC112. Examiner rejected claims 1-16 (all the claims) in view of Zhu US 5,866,924 variously under 35USC102 and 35USC 103. For example, claim 1 was rejected under the provisions of 35USC102, based on Examiner's contention that all the elements of the claim are met by Zhu. Other claims were rejected under the provisions of 35USC103, as for example claim 2, with the explanation that: "Zhu does not show the receiver (sink) but such a receiver must exist in order for the clocks to be useful". In addition, claim 8 was rejected under 35USC103 as being unpatentable over Zhu in view of Ryum et al, US 5,981, 345. Ryum was cited for the disclosed SiGe technology. Claims 6 and 14 were also rejected under 35USC103 as being unpatentable over Zhu in view of Sharpe-Geisler US 6,353,352. The Sharpe-Geisler patent was cited for disclosing: 1. "A

plurality of transmission lines configured to cancel noise" and 2. "Shielding". Applicant has canceled claims 1-16.

In order to more succinctly set forth the invention, applicant has added claims 17-24. Claim 17 now recites:

A clock signal distribution device formed on a semiconductor substrate 100, comprising:

a clock input 110;

a first driver 140 coupled to said clock input 110;

a second driver 150 coupled to said clock input110;

a first receiver 200 coupled to said first driver 140 by a first plurality of transmission lines 180;

a second receiver 210 coupled to said second driver 150 by a second plurality of transmission lines 190;

said first and second plurality of transmission lines being configured to provide substantially equal time delays;

said first receiver 200 configured to provide a first output 120 connected to a first site on a microprocessor 300; and

said second receiver 210 configured to provide a second output 130 connected to a second site on said microprocessor 300.

Exemplary reference numerals from the drawing figure have been added to facilitate explanation of the patentable distinctions and not by way of limitation. It is noted that although Zhu and applicant address the same problem, the structure and mode of operation of the two inventions are patentably distinct. With reference to FIG. 9 of Zhu, there is disclosed a semiconductor device 900a incorporating a local clock tree, a package 970 incorporating a global clock tree 950 and an integrated circuit 900b receiving synchronized clock signals from the global clock tree and also incorporating a local clock tree. The global clock tree is an inherent part of the Zhu invention because:

"the resistance of the package layer interconnects is 2-3 orders of magnitude less than that of the integrated circuit layers" (column 10 lines 21-23).

With continued reference to FIG. 9, it is noted that solder bump 940a on chip 900a corresponds to solder pad110 in applicant's claim 1. Following this line of analogies, then clock source 910 is the equivalent of applicant's first driver 140. In applicant's invention, driver 140 is connected to first receiver 200 by a plurality of transmission lines. Receiver 200 then provides an output to external circuitry (the microprocessor) via solder bump 120. In contradistinction, the output of 910 in FIG. 9 is routed to solder bump 940a to the global clock tree 950 and then somehow back to integrated circuits 900a and 900b.

It is noted that in order to analogize the Zhu patent with applicant's invention, Examiner states that solder bumps 940c-i are the equivalent of applicant's clock input 110. Then, a buffer in1030a (FIG.10B) becomes the equivalent of first driver 140. Examiner further notes that: "Zhu does not show a receiver (i.e. receivers 200 and 210 in the instant application) but such a receiver must exist in order for the clocks to be useful." But, in fact, Zhu's buffers might provide signals directly to a utilization circuit, in which case, there would be no receiver between the "buffers" and the utilization circuit, e.g. microprocessor. One can only speculate because the receivers (an important feature in applicant's invention) are not shown at all in Zhu. Moreover, in addition to the receivers, Zhu also fails to teach solder bumps 120 and 130 which form the output of the chip and are then connected to multiple sites on microprocessor 300. These missing elements from Zhu are more than mere design choice. Rather, Zhu contemplated a structure where the utilization circuits and local clock trees are on the same semiconductor substrate, with a global clock tree in the package. Zhu never contemplated the invention of applicant, which uses a clock distribution device that provides two or more synchronized pulses to a utilization device, e.g. a microprocessor.

Thus, there is no teaching whatsoever in Zhu for the last two paragraphs in claim 17, to wit:

said first receiver 200 configured to provide a first output 120 connected to a first site on a microprocessor 300; and

said second receiver 210 configured to provide a second output 130 connected to a second site on said microprocessor 300.

Accordingly, claim 17 is believed to be allowable. Claim 18 is also believed to be allowable for the same reasons and further that it identifies the semiconductor substrate as comprising silicon germanium. This further clarifies the fact that the clock signal distribution device 100 and utilization device are on separate substrates. Typically, microprocessors are fabricated on silicon substrates. By putting the clock signal distribution circuits and utilization circuits on the same silicon substrate, as was done in the prior art, e.g. Zhu, the advantages of applicant's invention would not be realized. Moreover, the general knowledge that silicon germanium devices can be faster than silicon devices, as taught in Ryum US 5.981.345, does not render applicant's invention obvious. Until applicant's invention, no one conceived of using a SiGe clock signal distribution chip for generating multiple synchronized clock signals to distinct sites on a microprocessor. Moreover, merely running conductors to multiple sites on a microprocessor would not achieve the same result. Receiver 200 provides power to the microprocessor at the site where it is connected independent of the power requirements of any other site that might be connected to the output of receiver 210 or any other receivers that might be utilized.

Claim 19, depending from claim 17 is believed to be allowable for the same reasons and that it recites a plurality of transmission lines that are configured to transmit both in phase and out of phase signals. Since Zhu does not show receivers, Zhu also fails to show this particular connection to the receivers.

Claim 20, depending from claim 17 is believed to be allowable for the same reasons and that it recites the clock input as a solder bump. Although Zhu discloses this detail, claim 20 is believed to be allowable because it depends from an allowable claim.

Claim 21, depending from claim 17 is believed to be allowable for the same reasons and that it recites first and second outputs configured as solder bumps. As was previously noted, Zhu discloses a clock tree on the same chip with the utilization devices and therefore the outputs are not solder bumps. Solder bump 940b in FIG. 9 is an output but it is only one output and is not connected at an analogous circuit point.

Claim 22 is another claim submitted to more succinctly claim Applicant's invention. Claim 22 recites:

An integrated circuit device formed on a semiconductor substrate and configured to provide synchronized clock signals to multiple sites on a utilization device located external to the semiconductor substrate, comprising:

a clock input configured as a solder bump;

a first driver coupled to said clock input;

a second driver coupled to said clock input;

a first receiver coupled to said first driver by a first plurality of transmission lines;

a second receiver coupled to said second driver by a second plurality of transmission lines;

said first and second plurality of transmission lines being configured to provide substantially equal time delays;

said first receiver configured to provide a first output connected to a first site on a utilization device; and

said second receiver configured to provide a second output connected to a second site on said utilization device.

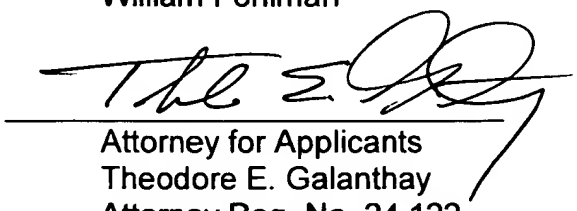
wherein said first and second outputs are configured as solder bumps connected to first and second sites on said utilization device.

As previously noted, Zhu does not teach a clock signal distribution device that provides, as an output, a plurality of synchronized clock pulses to a device external to the clock signal distribution device. For this reason, the structural combination and function of claim 22 are not disclosed by Zhu. For the reasons described herein, claim 22 is believed to be allowable. Claim 23 depends from claim 22 and is believed to be allowable for the same reasons and that it further recites a germanium substrate, which in the overall combination is believed to provide additional patentable import.

Claim 24 depends from claim 22 and is believed to be allowable because it depends from an allowable claim. Moreover, claim 24 specifically recites that the utilization device is a microprocessor.

In view of the foregoing, it is believed that claims 17-24, all the claims currently in this application, are in condition for allowance. If Examiner has a question or comment or if Applicants' attorney can assist in any manner whatsoever, Examiner is respectfully requested to telephone the undersigned. An early notification of allowance is earnestly solicited.

Respectfully submitted,
William Pohlman



Attorney for Applicants
Theodore E. Galanthay
Attorney Reg. No, 24,122

From: Primarion, Inc.
2507 W. Geneva Drive
Tempe, Arizona 85282

Telephone: 480-575-0744

TEG/cw